alpitronic

PCTB

Power Cycling Testbench for Power Electronic Modules

PC-LAB

Power Cycling Test Laboratory


alpitronic

Technical Information

PCTB power cycling test bench

alpitronic has many years of experience in developing power cycling test benches and in carrying out power cycling tests for customers according to the standard IEC 60749-34 and the automotive standard LV 324. This experience is based on the successful cooperation with leading semiconductor manufacturers and automotive OEMs.

PCTB KEY FEATURES

- contemporaneous testing of up to 12 IGBT, Diode or MosFET power modules
- load currents up to 1200A
- cooling temperatures from 25°C to 120°C
- easy connection of the DUTs regardless of the package type
- measurement of the thermal impedance and the thermal resistance
- coolant flow individually adjustable for each device under test
- interrupt of cooling flow during heating for PCmin tests
- power cycling tests compliant to IEC 60749-34 and automotive standard LV 324

OVERVIEW

Power cycling tests are accelerated lifetime tests for power electronic modules which stress the module's assembly and contact mechanisms. The modules' lifetime is reached by the progressive fatigue of the module due to repetitive thermo-mechanical stress. The thermomechanical stress is induced by periodically heating up the module with a load current through the tested semiconductors and by cooling the module down after load current switch-off. The module's lifetime, expressed in number of power cycles until failure, mainly depends on the semiconductor's junction temperature swing, mean junction temperature and the heating time which are characteristic parameters for a power cycling test. From the test results, a lifetime model for the tested module type can be derived which is a key component for assessing the module's lifetime in a given application.

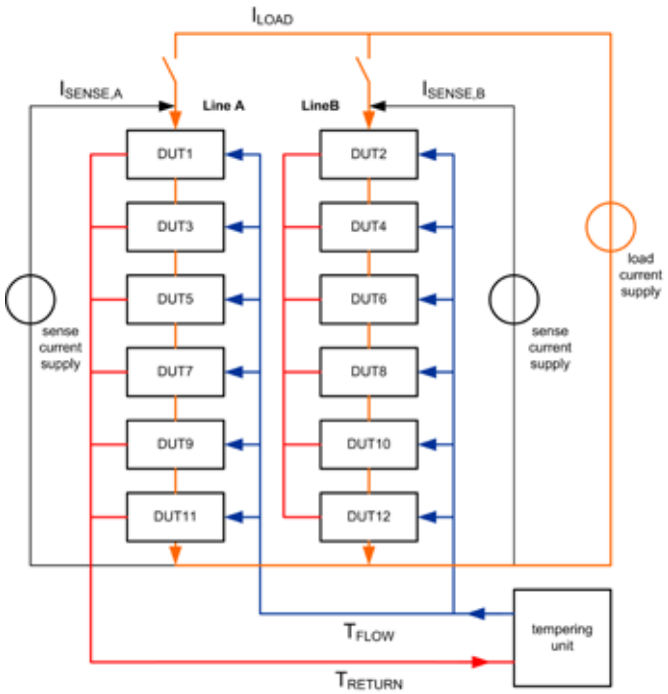
On the alpitronic PCTB power cycling test bench, up to 12 half bridges can be tested for power cycling lifetime at the same time. The modules are connected in series on two test lines which are alternately stressed by applying a load current of up to 1200A, thus allowing a very efficient utilization of the installed load current supplies. Each DUT is connected to the load current circuit by a low impedance busbar and has a dedicated measurement and control unit which communicates with a central control unit. This allows a very flexible handling of the numbers of modules tested. The DUTs can be mounted on up to 12 cooling plates which are connected in parallel to the

cooling circuit by fast couplings. The standard cooling plates can easily be replaced by custom cooling plates which are necessary when testing pin-fin modules. The cooling circuit provides a wide flow temperature range from 25° to 120°C. Besides performing power cycling tests, the test bench can also be used to determine the thermal impedance and the thermal resistance of power cycling modules.

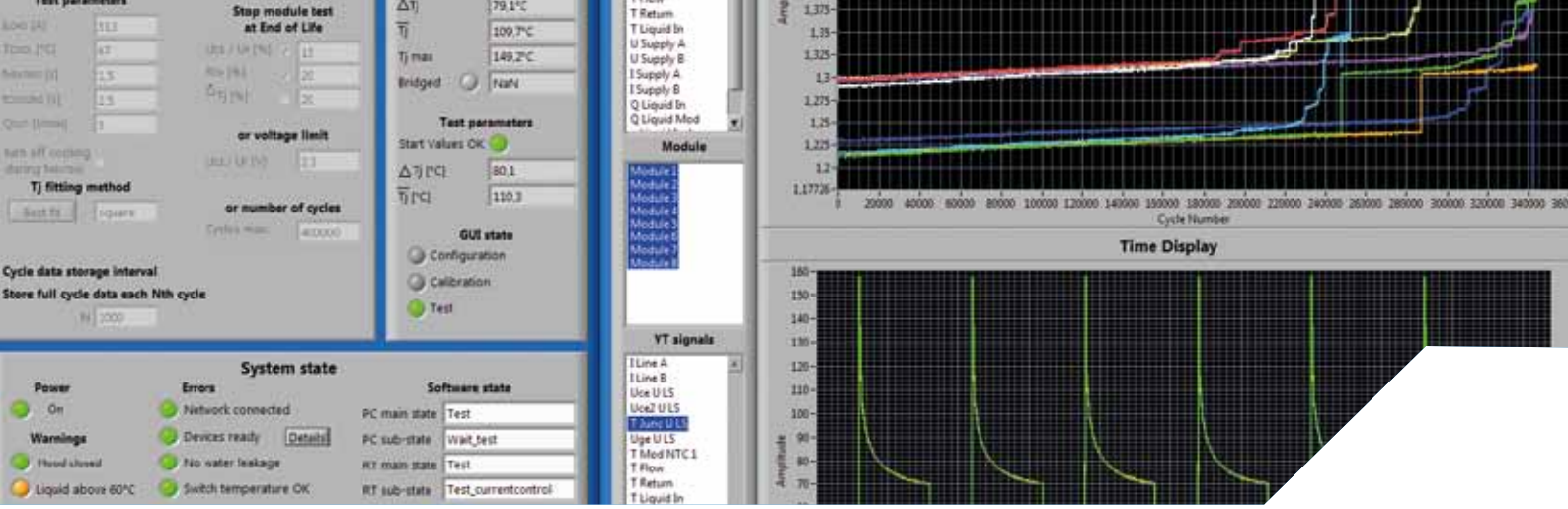
The implemented power cycling test control algorithm keeps the load current, the heating time and the cooling time constant during the test. Among the various control strategies (e.g. constant junction temperature swing, constant heating power), the constant cycle time control strategy is the control strategy closest to application and stresses the modules most which leads to short test times.

Before a power cycling test is started, a calibration curve describing the dependency of the junction temperature of the conduction voltage at an adjustable sense current is recorded for all tested semiconductors. Thus, the junction temperature of each tested semiconductor can be determined during the cooling phase of each power cycle by measuring the conduction voltage at the chosen sense current. The maximal junction temperature at the end of the heating phase is measured already 100us after turning off the load current.

At test start, the start values for conduction voltage, thermal resistance and junction temperature swing are recorded of each switch as soon as they have stabilized. From the start values, the characteristic test parameters junction temperature swing ΔTj and mean junction temperature T_m are derived. At each cycle, end of life conditions are monitored for each DUT. As failure criteria, a percentage limit for the increase of the conduction voltage, of the thermal resistance and / or of the junction temperature swing can be selected by the user. For each power cycle, characteristic cycle parameters like conduction voltage, thermal resistance, maximum and minimum junction temperatures and several other measurement data are recorded. When a DUT fails, the test is continued with the remaining DUTs after bridging the failed module.

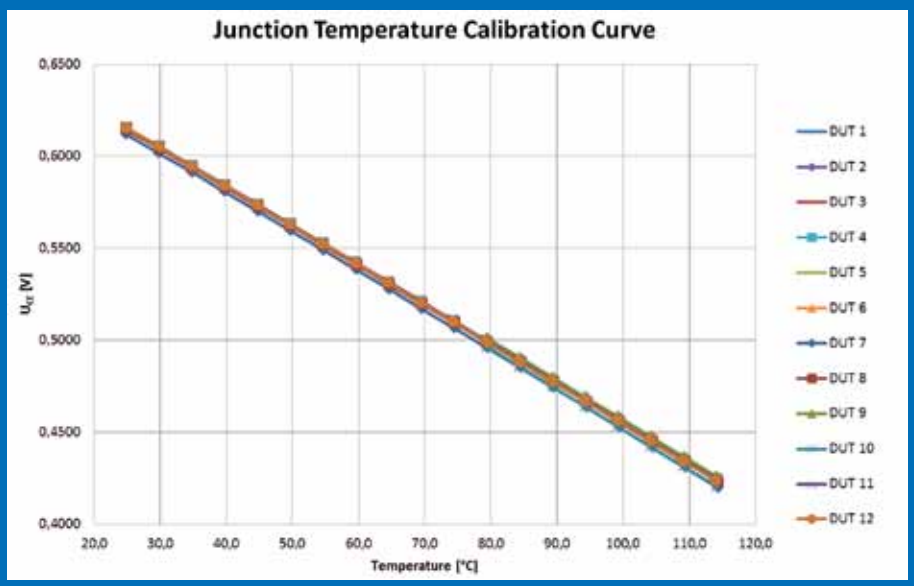


For each DUT, two data records are saved. The first data record comprehends all characteristic cycle values for each cycle over lifetime, while the second data record saves the measurement signals of an entire cycle with 20Hz resolution for selected cycles over lifetime. When the thermal impedance option is chosen, a third data record is generated which contains the high resolution thermal impedance curve (up to 20kHz) for selected cycles over lifetime.



CALIBRATION

Before the power cycling test is started, all tested semiconductors are calibrated individually to record the almost linear dependency between conduction voltage and junction temperature at a specified sense current. The conduction voltage is measured at different, user configurable temperature points from 25°C to 120°C. The semiconductor's conduction voltage is recorded at each temperature point after the module has reached a thermal steady state, assuming that the semiconductor's junction temperature is equal to the measured flow temperature. Junction temperatures above the recorded temperatures are extrapolated either with a linear or with a quadratic approximation. For semiconductors with noticeable nonlinear temperature dependency above the maximum recordable calibration temperature of 120°C, calibration data can be also recorded externally (e.g. in a temperature chamber) and loaded into the application.



Technical Information

PCTB power cycling test bench

TEST SETUP AND MONITORING

Power cycling tests can be configured and monitored by an intuitive and easy to use control application. Following information has to be inserted by the user to configure a test:

- General information: test description, module type, module information
- DUT settings: name of each DUT, position on test bench
- Temperature settings: number of module NTCs to be read (0-2), number of external (e.g. heat sink) temperature sensors to be read (0-2), Rth reference temperature selection, tested semi conductor type
- Calibration settings: calibration temperatures, sense current, gate voltage
- Test settings:
    - o Test parameters: load current, heating time, cooling time, coolant temperature, coolant flow
    - o End of life conditions: limits for conduction voltage increase, temperature swing increase

It's also possible to load the test configuration of a previous test into the application by opening or importing that test. When a test is opened, also the measurement data are loaded to a display on the right side of the application.

During the power cycling test, the module's status can be observed by two graphs in the control application. The upper graph shows characteristic cycle values like conduction voltage, thermal resistance, maximum or minimum junction temperature as a function of the cycle number. The lower graph shows the measured signals of the actual cycles at a sample rate of 20Hz.

A status display at the left of the graphs shows the numbers of the start values and the actual values of conduction voltage, thermal resistance and maximum value, mean value and swing of the junction temperature for each tested switch.

Technical Information

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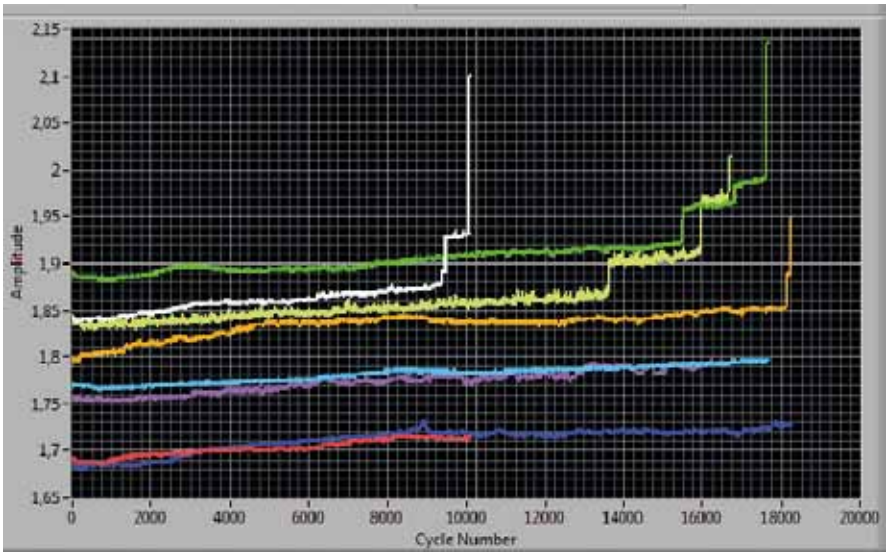
FAILURE ANALYSIS

At the end of the power cycling test, a first failure analysis can be done by evaluating the failure criteria. When the lifetime is reached due to the increase of the conduction voltage, the failure cause is prevalently a degradation of the bond wires, visible by voltage steps in the voltage signal. When the increase of the thermal resistance or the junction temperature swing determines the lifetime, the failure is probably caused by a degradation of the solder layers in the heat conduction path, e.g. a degradation of chip solder.

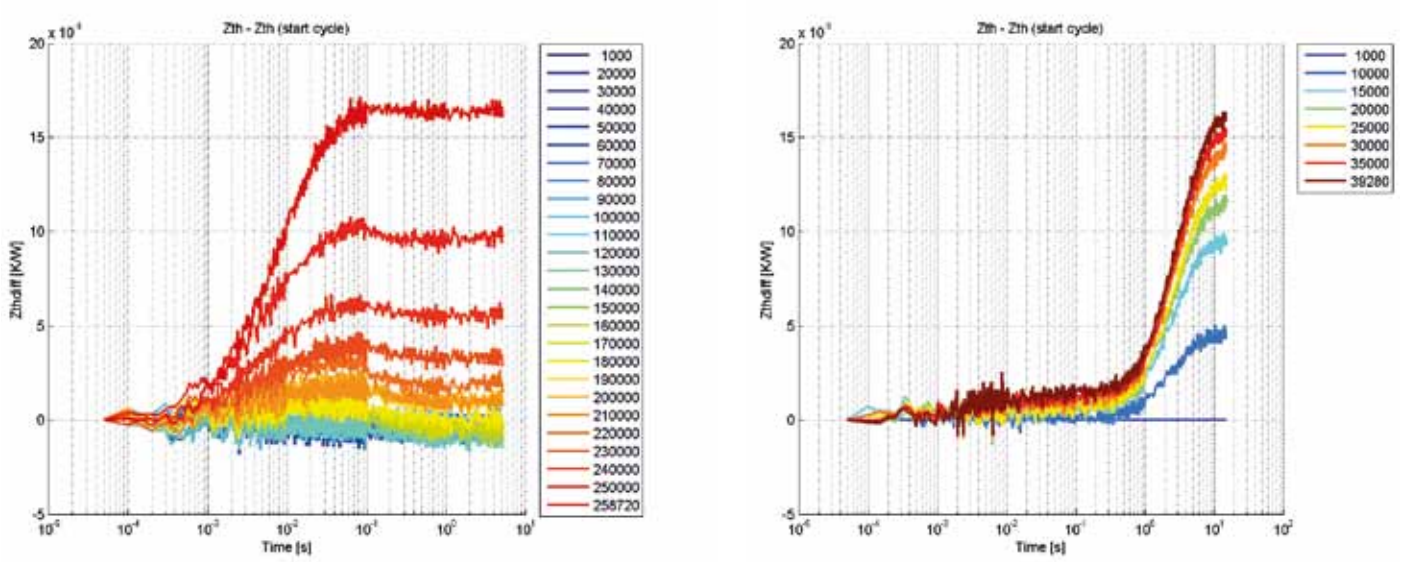


THERMAL IMPEDANCE MEASUREMENT

Failure analysis can be further improved by optionally recording the thermal impedance curve of the DUTs during the cooldown phase. The thermal impedance is recorded with up to 20 kHz resolution. By analyzing the changes in thermal impedance over lifetime, the degradation of the thermal interface can be locally assigned to the different layers of the module (e.g. chip solder, system solder or thermal interface material). If the increase of the thermal impedance occurs early in the thermal response (e.g. before 100ms), it's commonly caused by degradation of the chip solder. Deviations at a later time can be assigned to system solder degradation (around 500ms) or to TIM degradation (> 1s). The given times are only indicative and depend on the module topology. The picture on the top right shows the deviation of an IGBT's thermal impedance curve from the start curve during two different power cycling tests. In the first test (on the left), the increase of the thermal impedance was caused by a the degredation of the chip solder while in the second test (on the right), it was caused by a baseplate delamination.

During a power cycling test, the chosen heating times are in the majority of the cases not long enough to get a thermal steady state of the module. Therefore, the thermal impedance curve recorded during the power cycling tests serves only for comparative evaluations.

For stand-alone measurements of a thermal impedance curve, the heating and cooling times have to be chosen long enough to guarantee a thermal equilibrium at the end of the heating phase and the cooling phase.



Deviation of thermal impedance over lifetime caused by degradation of the chip solder (left) and a baseplate delamination (right)

PCMIN FUNCTIONALITY

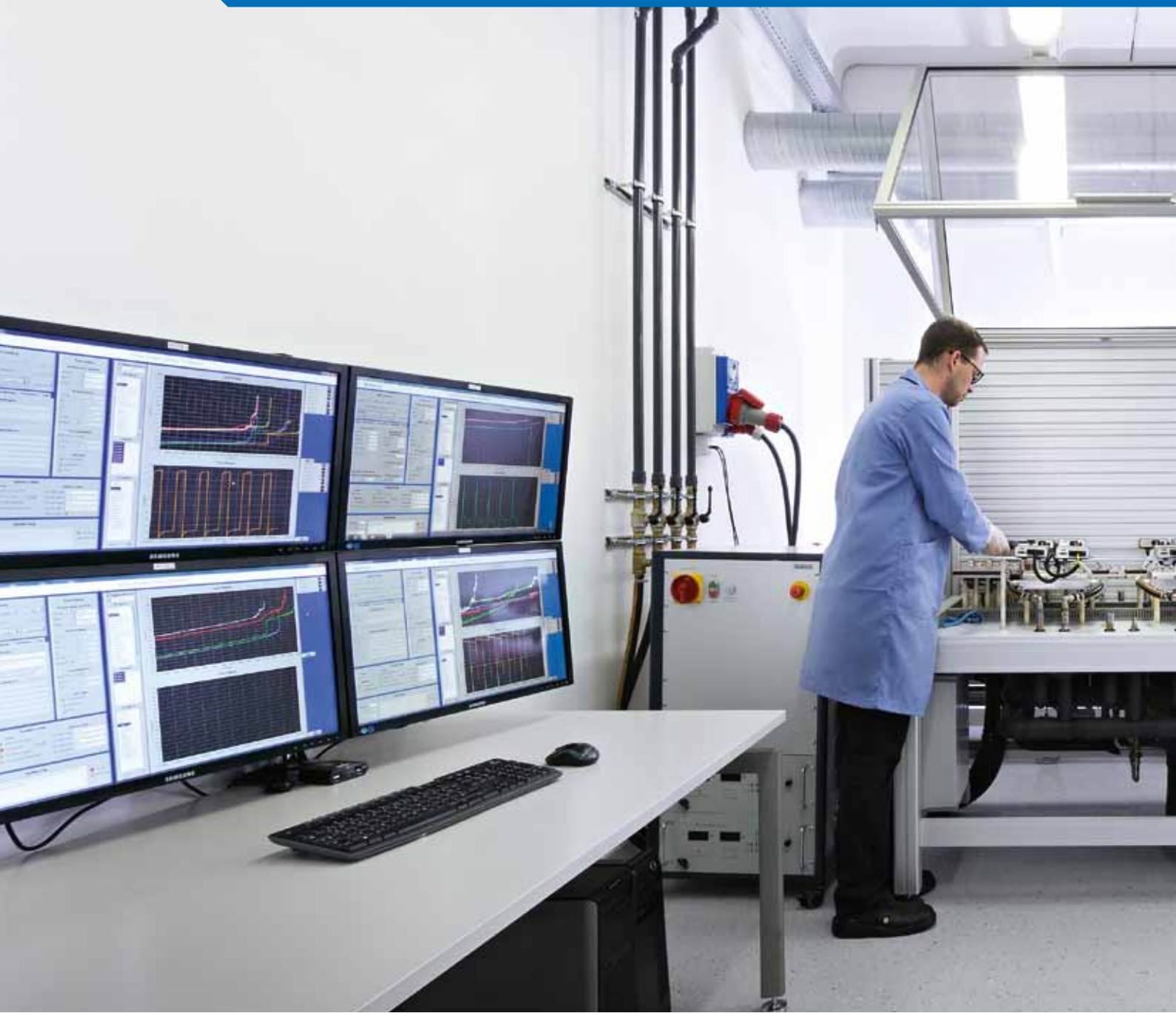
The power cycling standards distinguish between power cycling test with short heating times < 15s (PCsec) and long heating times (PCmin). PCsec tests exercise thermomechanical stress on chip-near interconnections like die attach and top connections, while PCmin tests stress at the same time the chip-remote interconnection technology like system soldering. For PCmin test, a certain swing of the module case temperature is required. To achieve the required temperature swing of the case temperature with reasonable heating times, the test bench can optionally interrupt the cooling flow through the heatsink at PCmin tests during the heating phase. This enables a faster rising of the case temperature.

INDIVIDUAL COOLING FLOW ADJUSTMENT

In the standard configuration of the test bench, a sophisticated hydraulic concept is used to achieve the same cooling flow through all of the heatsinks connected in parallel to the cooling circuit. In order to guarantee exactly the same cooling conditions for each module, the flow to each heatsink can be optionally measured by a dedicated flow sensor and tuned manually by a valve in the conduction path.

PC-LAB power cycling test lab

alpitronic's power cycling test lab offers power cycling test capacities to carry out in-house power cycling tests for customer modules. The test lab is audited by a leading semiconductor manufacturer in order to perform production qualification tests. Power cycling tests are carried out according to IEC 60749-34 or to the automotive standard LV 324 in close coordination with the customer.



In-house power cycling tests for customer modules are prepared by planning the interface of the modules to the load current circuit, the cooling circuit and to the control and measurement interface. Before starting the power cycling test, the dependency of the conduction voltage by the junction temperature is recorded either on the test bench or in a temperature chamber, thus allowing an unlimited temperature range for recording. The setup of the test parameters required to achieve the requested junction tempera-

ture swing and mean value is determined by the lab technician and released by the customer. During the test, the customer is updated on the test process by periodic short reports.

After completion of the test, the tests results are comprehensively analyzed and documented by a test report. Failure analysis can be enhanced by additional non-destructive analysis methods like optical inspection at open housing, X-ray or Scanning acoustic microscopy (SAM) for which we rely on external partners.

PCTB TECHNICAL DATA

Tester Type	PCTB-D-800-15	PCTB-D-1200-15	PCTB-D-600-30	PCTB-D-800-30
Number of DUTs	up to 8 half bridges		up to 12 half bridges	
DUT Types	single switch, half bridge, H-bridge, B6 bridge			
Semiconductors	IGBTs, diodes, MOSFETS			
Supply Voltage of Load Current Circuit	15 V		30 V	
Load Currents	10 - 800 A	10 - 1200 A	10 – 600 A	10 – 800 A
Sense Current	10-200 mA			
Heating Time	0,5 s-150 s			
Cooling Time	0,7 s-150 s			
Gate Voltage	-8 V-20 V			
Cooling flow (sum flow)	5-90 l/min			
Coolant type	50% water ethylene glycol			
Cooling temperature range	25°C – 120°C			
End of Life criteria (selectable)	raise of: conduction voltage, Rth or $\Delta T_{Junction}$			
Recorded Data	conduction voltage, junction temperature, thermal resistance, load current, Module-NTC-temperatures, cooling plate temperatures, inlet and outlet cooling liquid temperatures on each DUT, cooling flow, cooling liquid pressure			
Dimensions (WxHxD)	Test bed: 165 x 185 x 115 cm Test rack: 55 x 121 x 80 cm		Test bed: 225 x 185 x 115 cm Test rack: 55 x 121 x 80 cm	
Mains Supply	3 x 400 V~, 64 A, 50 Hz			
Building site cooling	Water, < 20°C, 4 bar			
Options				
thermal impedance measurement (stand-alone /during power cycling test)				
PCmin functionality (interruption of cooling-flow during load current phase)				
individual cooling flow adjustment (measurement and manual cooling-flow regulation for each DUT)				

Our engineering department is working continuously at the improvement of our test benches.
We will be glad to implement special requirements or a customized solution.

For further information please contact:

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